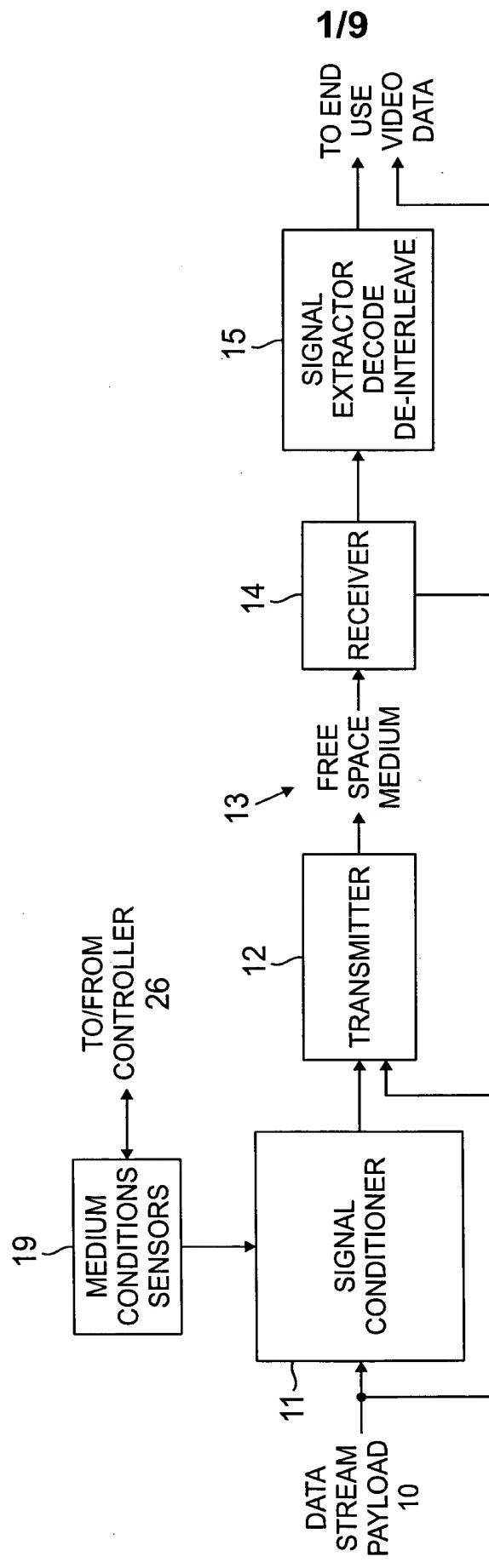
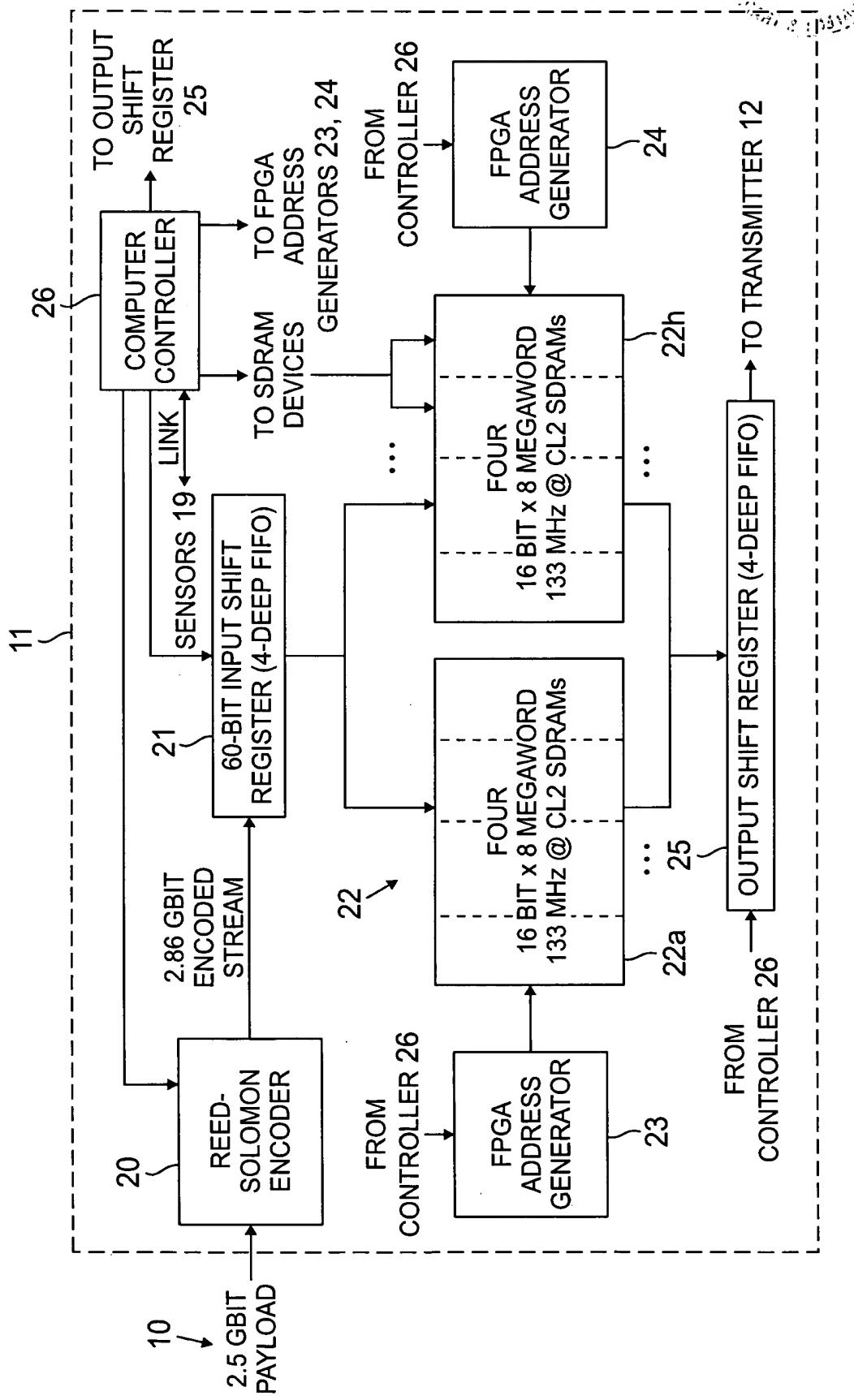
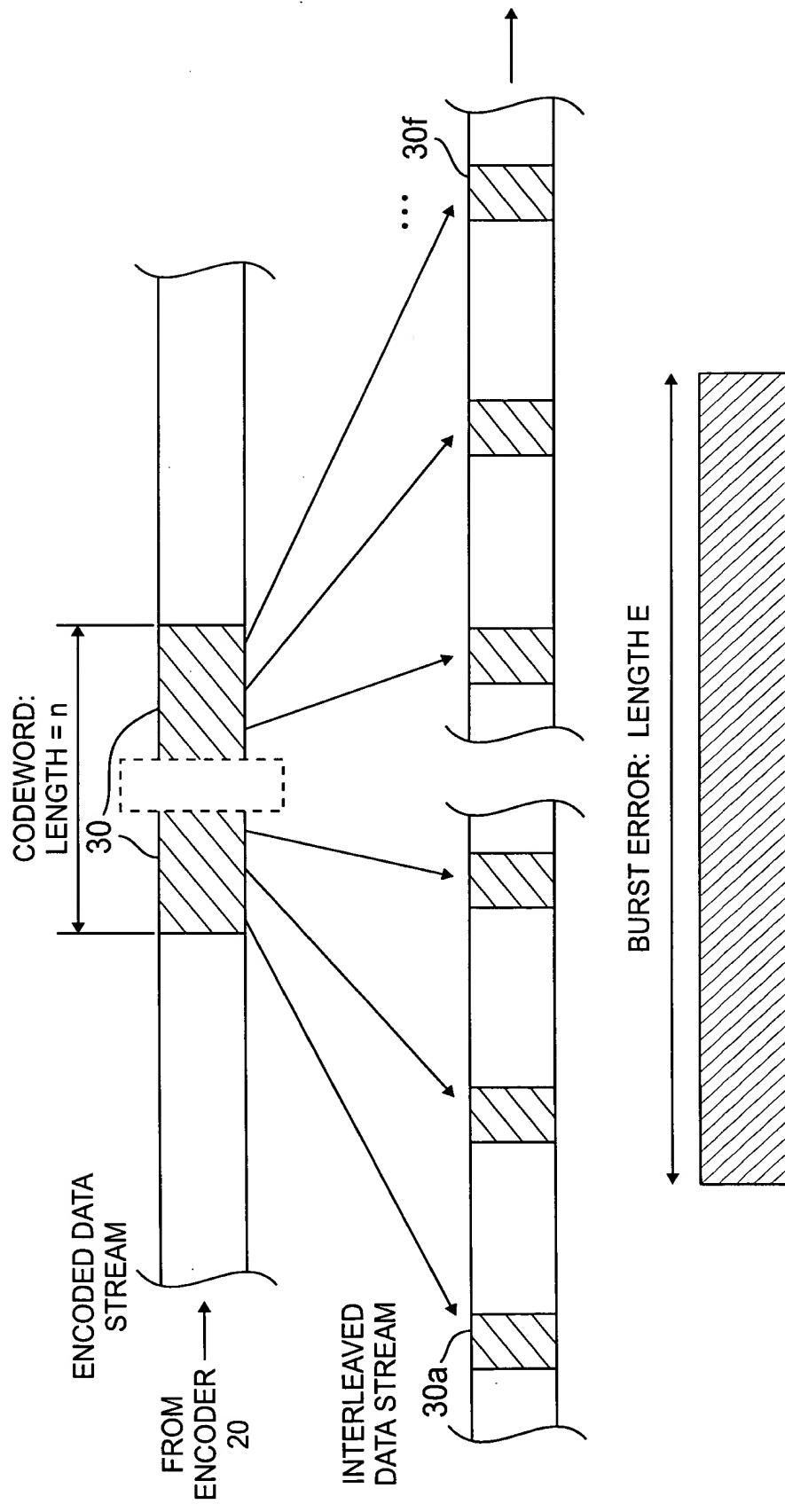


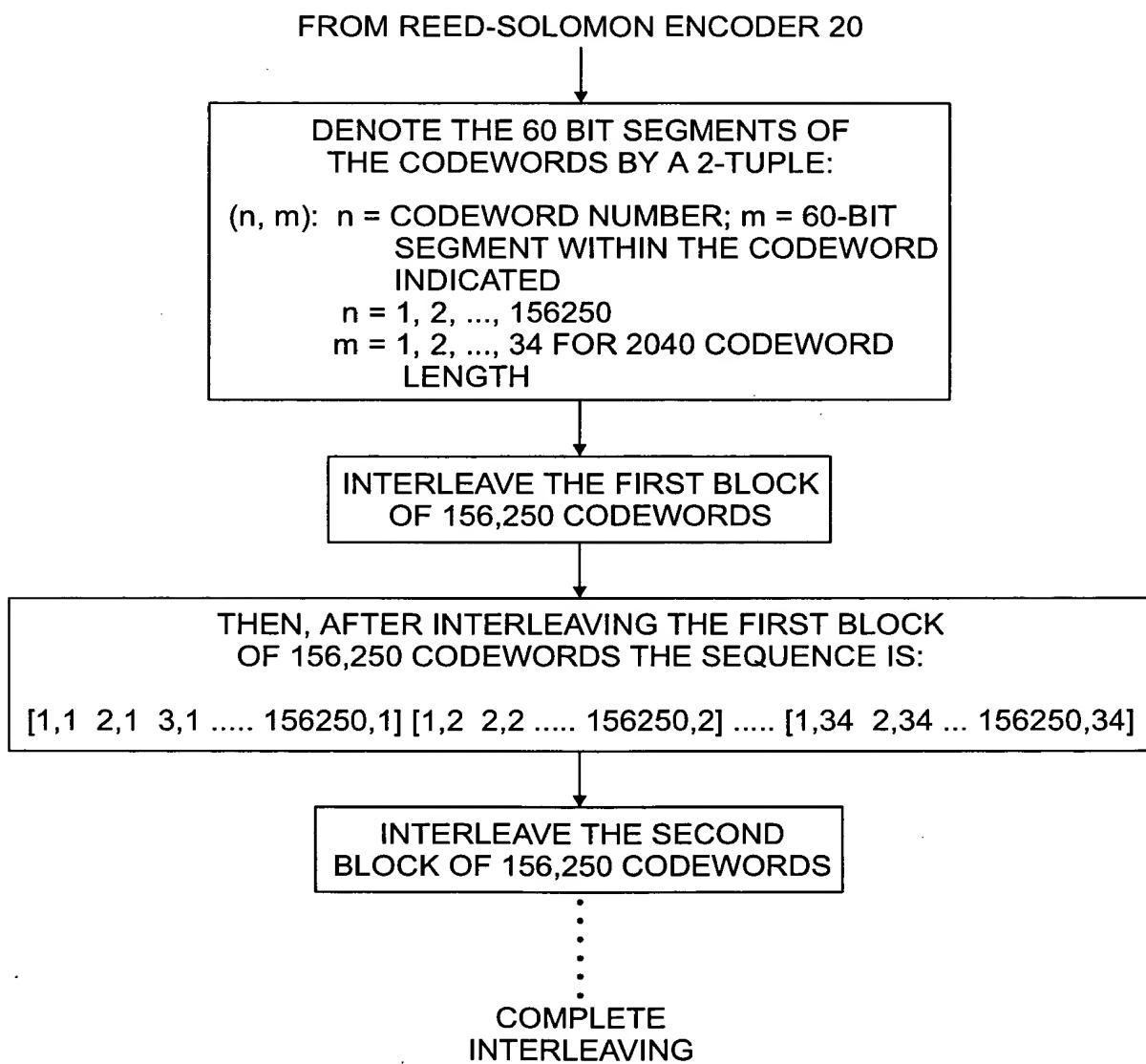
FIG. 1

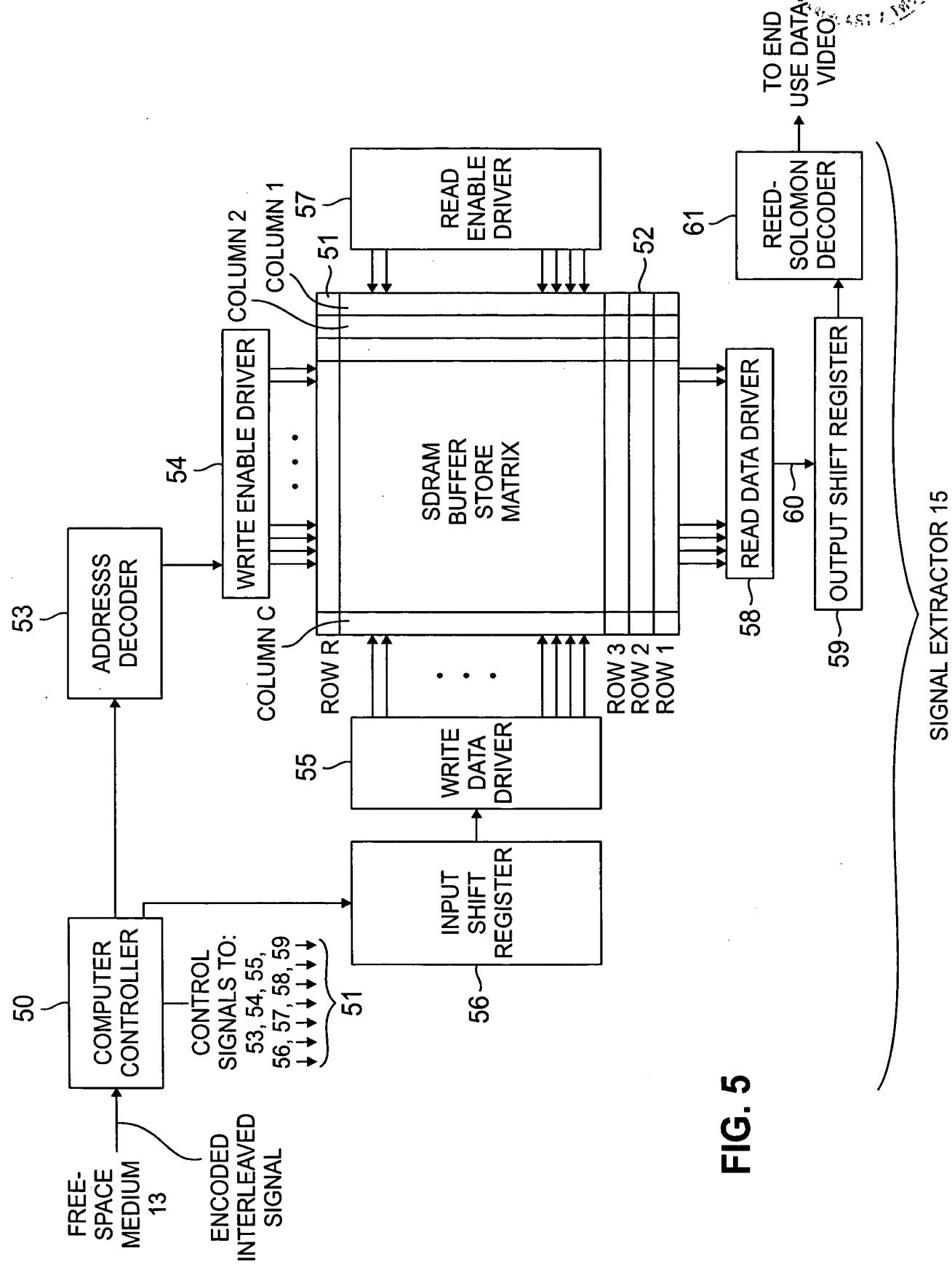


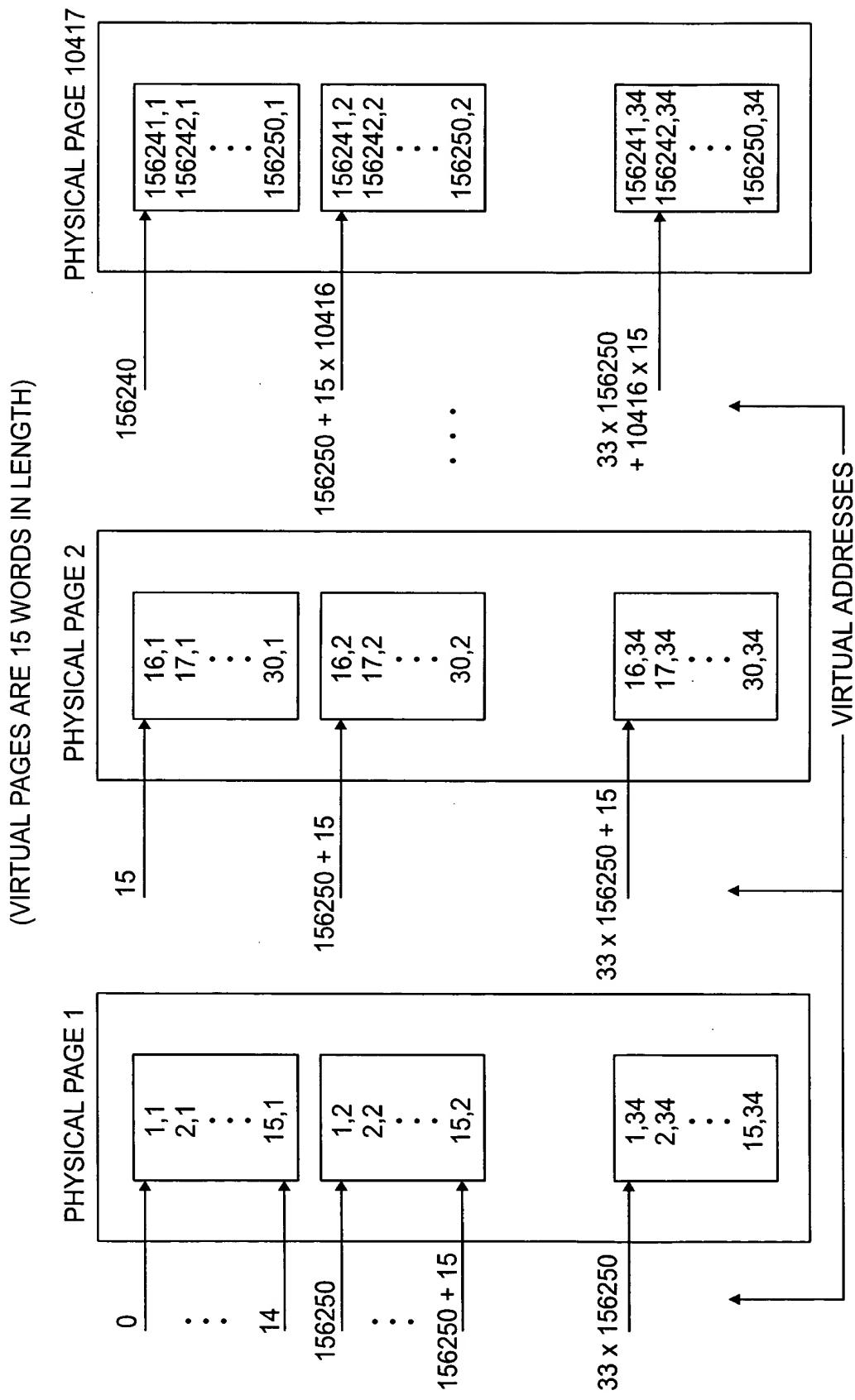
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**FIG. 2**

**FIG. 3**

**FIG. 4**



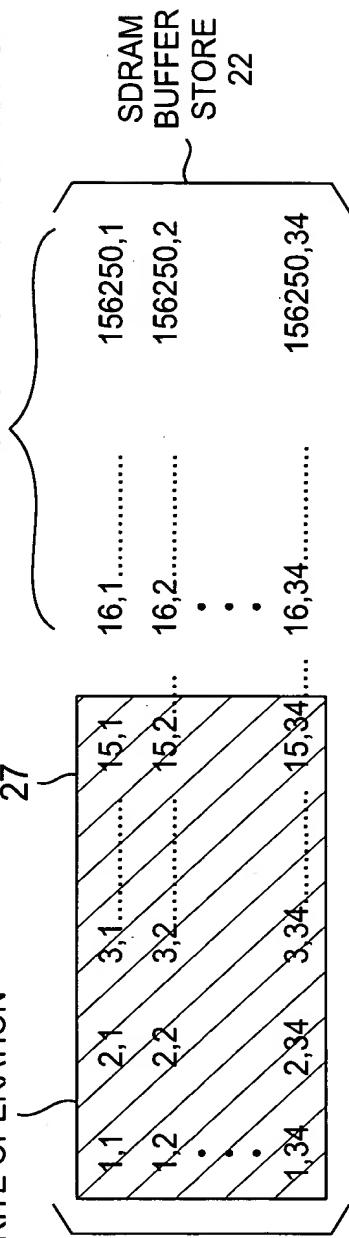


REMAPPING ADDRESSES TO BALANCE
"READ" VS. "WRITE" OVERHEAD IN TERMS
OF SDRAM PAGE CHANGES

FIG. 6A

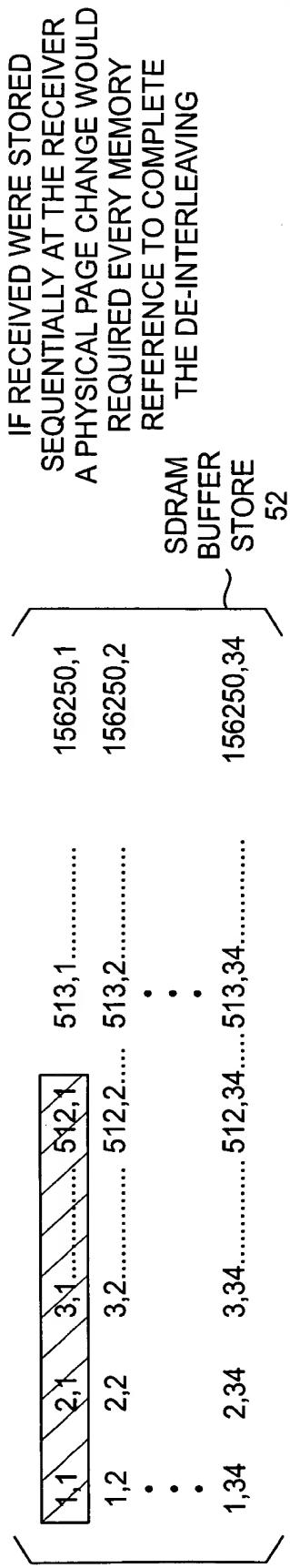
SUB-MATRIX MAPPING 60-BIT ENTRIES INTO FIRST DRAM PAGE OF 512 ADDRESSES, USING 510 MATRIX CELLS TO STORE FIRST CODEWORD DURING WRITE OPERATION

SUCCESSIVE ADDITIONAL (APPROX. 10,416) SUB-MATRICES MAPPING FURTHER 60-BIT ENTRIES INTO SDRAM PAGES TO STORE SECOND THROUGH m^{th} CODEWORDS DURING WRITE OPERATION

**FIG. 6B**

CODEWORD SEGMENTS EXPRESSED AS A MATRIX

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CROSS-HATCHED SUBMATRIX INDICATES SEGMENT OF RECEIVED MATRIX THAT WOULD BE HELD ON ONE 512 ADDRESS PAGE IF RECEIVER STORED ENTRIES SEQUENTIALLY

FIG. 6C

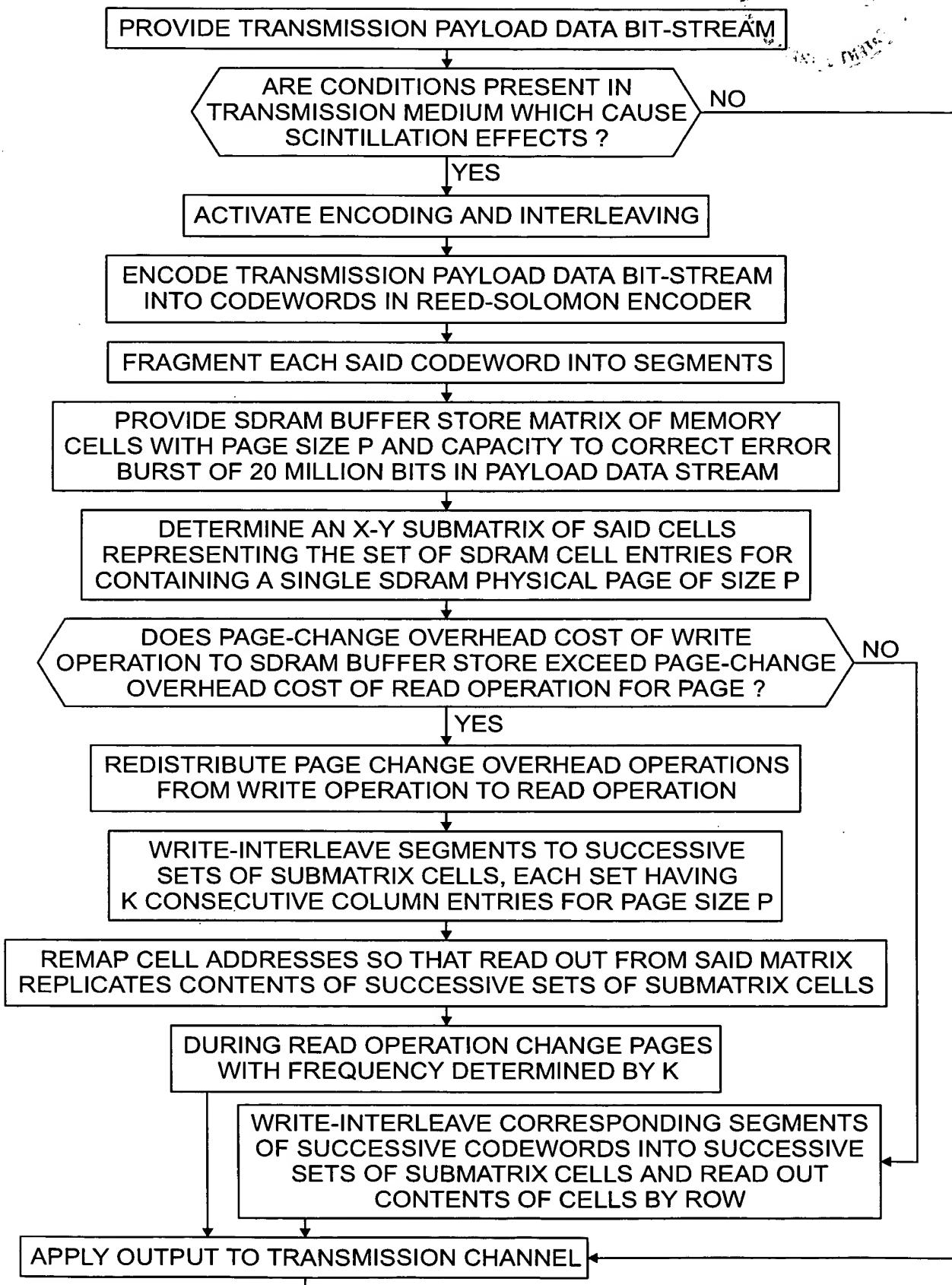
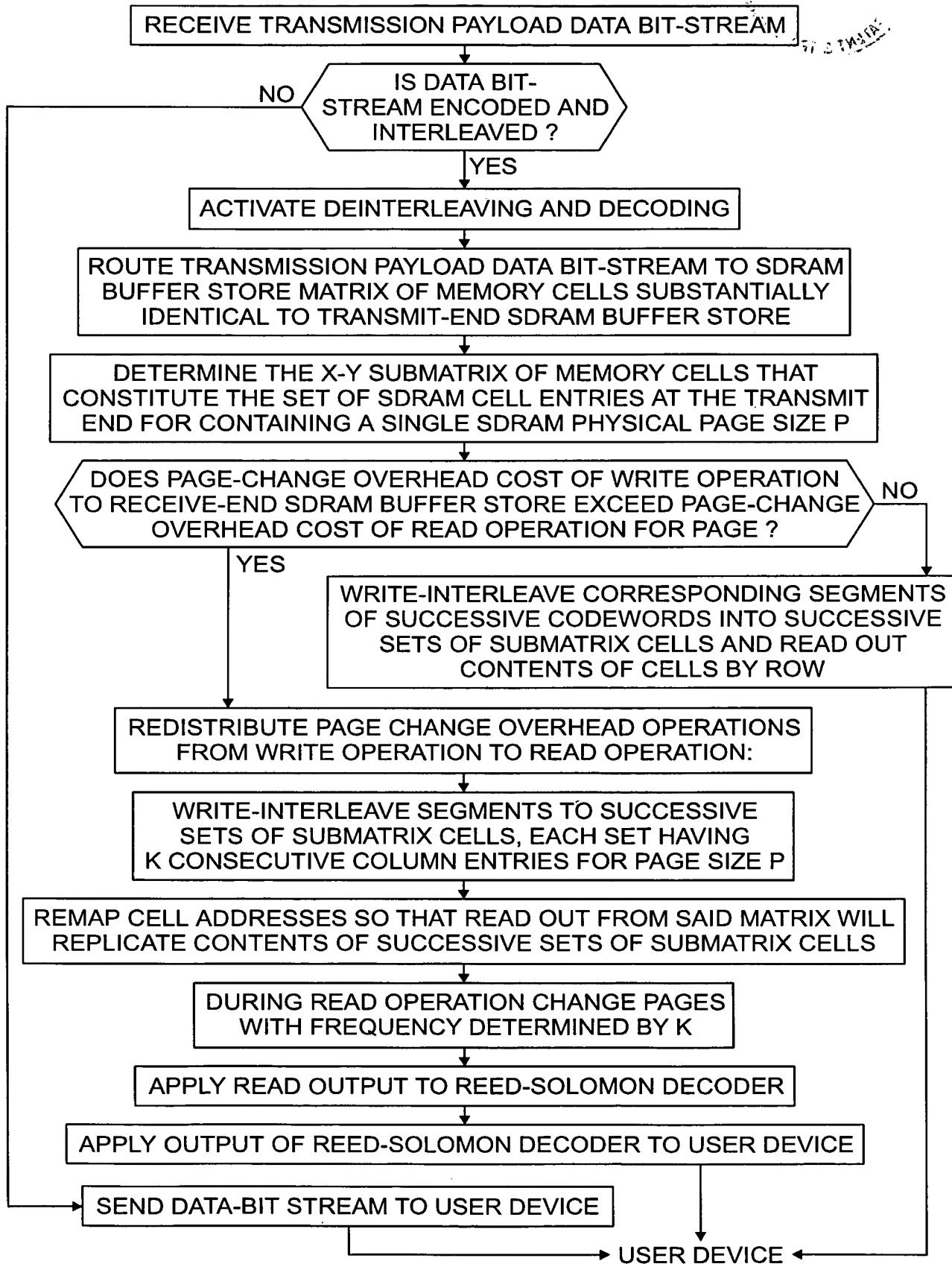


FIG. 7A

FLOW CHART OF PROCESS
AT TRANSMITTER END



FLOW CHART OF PROCESS AT RECEIVER END

FIG. 7B